What is Claimed Is:

1. An ESD protection apparatus installed between a pad of a semiconductor integrated circuit chip and an inner circuit of said semiconductor integrated circuit chip, comprising:

a trigger element having a diode to be broken down by overvoltage applied to said pad; and

an ESD protection element having a longitudinal bipolar transistor for discharging the accumulated electric charge of said pad by being electrically communicated attributed to the breakdown of said diode.

2. The ESD protection apparatus according to Claim 1,

wherein said diode comprises a single diode or plural diodes connected in series;

said overvoltage is a forward voltage for the diode; and

said breakdown is a substantial breakdown owing to conduction.

3. The ESD protection apparatus according to Claim 1, wherein said pad is an input terminal or an output terminal;

said trigger element comprises a first and a second diodes and a first and a second resistors;

said ESD protection element comprises NPN type first and second longitudinal bipolar transistors;

a cathode of said first diode is connected with said pad and an anode of said first diode is connected with a base of said first longitudinal bipolar transistor;

a cathode of said second diode is connected with an electric power source terminal and an anode of said second

diode is connected with a base of said second longitudinal bipolar transistor;

said first resistor is connected between the anode of said first diode and a ground terminal;

said second resistor is connected between the anode of said second diode and said pad;

a collector of said first longitudinal bipolar transistor is connected with said pad and an emitter of said first longitudinal bipolar transistor is connected with said ground terminal; and

a collector of said second longitudinal bipolar transistor is connected with said electric power source terminal and an emitter of said second longitudinal bipolar transistor is connected with said pad; and

at least either of said first diode, said first resistor and said first longitudinal bipolar transistor or said second diode, said second resistor and said second longitudinal bipolar transistor are provided.

4. The ESD protection apparatus according to Claim 1, wherein said pad is an input terminal or an output terminal;

said trigger element comprises first and second diodes and first and second resistors;

said ESD protection element comprises PNP type first and second longitudinal bipolar transistors;

a cathode of said first diode is connected with a base of said first longitudinal bipolar transistor and an anode of said first diode is connected with a ground terminal;

a cathode of said second diode is connected with a base of said second longitudinal bipolar transistor and an anode of said second diode is connected with said pad;

said first resistor is connected between the cathode of said first diode and said pad;

said second resistor is connected between the cathode of said second diode and said electric power source terminal;

a collector of said first longitudinal bipolar transistor is connected with said ground terminal and an emitter of said first longitudinal bipolar transistor is connected with said pad; and

a collector of said second longitudinal bipolar transistor is connected with said pad and an emitter of said second longitudinal bipolar transistor is connected with said electric power source terminal; and

at least either of said first diode, said first resistor and said first longitudinal bipolar transistor or said second diode, said second resistor and said second longitudinal bipolar transistor are provided.

5. The ESD protection apparatus according to Claim 1, wherein said pad is an electric power source terminal;

said longitudinal bipolar transistor is NPN type;

the cathode of said diode is connected with said pad and the anode of said diode is connected with the base of said longitudinal bipolar transistor;

a resistor is connected between the anode of said diode and a ground terminal; and

the collector of said longitudinal bipolar transistor is connected with said pad and the emitter of said longitudinal bipolar transistor is connected with said ground terminal.

6. The ESD protection apparatus according to Claim 1,

wherein said pad is an electric power terminal;

said longitudinal bipolar transistor is of PNP type;

a cathode of said diode is connected with a base of said longitudinal bipolar transistor and an anode of said diode is connected with a ground terminal;

a resistor is connected between the cathode of said diode and said electric power terminal; and

a collector of said longitudinal bipolar transistor is connected with said ground terminal and an emitter of said longitudinal bipolar transistor is connected with said pad.

7. The ESD protection apparatus according to Claim 2,

wherein said pad is an input terminal or an output terminal;

said trigger element comprises first and second diodes and first and second resistors;

said ESD protection element comprises NPN type first and second longitudinal bipolar transistors;

an anode of said first diode is connected with said pad and a cathode of said first diode is connected with a base of said first longitudinal bipolar transistor;

an anode of said second diode is connected with an electric power source terminal and a cathode of said second diode is

connected with a base of said second longitudinal bipolar transistor;

said first resistor is connected between the cathode of said first diode and the ground terminal;

said second resistor is connected between the cathode of said second diode and said pad;

a collector of said first longitudinal bipolar transistor is connected with said pad and an emitter of said first longitudinal bipolar transistor is connected with said ground terminal; and

a collector of said second longitudinal bipolar transistor is connected with said electric power source terminal and an emitter of said second longitudinal bipolar transistor is connected with said pad; and

at least either of said first diode, said first resistor and said first longitudinal bipolar transistor or said second diode, said second resistor and said second longitudinal bipolar transistor are provided.

8. The ESD protection apparatus according to Claim 2,

wherein said pad is an input terminal or an output terminal;

said trigger element comprises first and second diodes and first and second resistors;

said ESD protection element comprises PNP type first and second longitudinal bipolar transistors;

an anode of said first diode is connected with a base of said first longitudinal bipolar transistor and a cathode of said first diode is connected with a ground terminal;

an anode of said second diode is connected with a base of said second longitudinal bipolar transistor and a cathode of said second diode is connected with said pad;

said first resistor is connected between the anode of said first diode and said pad;

said second resistor is connected between the anode of said second diode and said electric power source terminal;

the collector of said first longitudinal bipolar transistor is connected with said ground terminal and the emitter of said first longitudinal bipolar transistor is connected with said pad;

the collector of said second longitudinal bipolar transistor is connected with said pad and the emitter of said second longitudinal bipolar transistor is connected with said electric power source terminal; and

at least either of said first diode, said first resistor and said first longitudinal bipolar transistor or said second diode, said second resistor and said second longitudinal bipolar transistor are provided.

9. The ESD protection apparatus according to Claim 2, wherein said pad is an electric power source terminal;

said longitudinal bipolar transistor is of NPN type;

an anode of said diode is connected with said pad and a cathode of said diode is connected with a base of said longitudinal bipolar transistor;

a resistor is connected between the cathode of said diode and a ground terminal;

a collector of said longitudinal bipolar transistor is connected with said pad and an emitter of said longitudinal bipolar transistor is connected with said ground terminal; and

at least either of said first diode, said first resistor and said first longitudinal bipolar transistor or said second diode, said second resistor and said second longitudinal bipolar transistor are provided.

10. The ESD protection apparatus according to Claim 2, wherein said pad is an electric power source terminal;

said longitudinal bipolar transistor is of PNP type;

an anode of said diode is connected with a base of said longitudinal bipolar transistor and a cathode of said diode is connected with a ground terminal;

a resistor is connected between the anode of said diode and said electric power source terminal;

a collector of said longitudinal bipolar transistor is connected with said ground terminal and an emitter of said longitudinal bipolar transistor is connected with said pad; and

at least either of said first diode, said first resistor and said first longitudinal bipolar transistor or said second

diode, said second resistor and said second longitudinal bipolar transistor are provided.

11. An ESD protection apparatus installed between a pad of a semiconductor integrated circuit chip and an inner circuit of said semiconductor integrated circuit chip, comprising:

a trigger element having a first longitudinal bipolar transistor whose collector and base act as a diode to be broken down by overvoltage applied to said pad and which discharges the accumulated electric charge of said pad by being electrically communicated due to the breakdown of the diode; and

an ESD protection element having a second longitudinal bipolar transistor for discharging the accumulated electric charge of said pad by being electrically communicated attributed to the breakdown of the diode.

12. The ESD protection device according to Claim 11,

wherein said pad is an input terminal or an output terminal;

said trigger element comprises an NPN type longitudinal bipolar transistor A and an NPN type longitudinal bipolar transistor B acting as said first longitudinal bipolar transistor, and a first and a second resistors;

said ESD protection element comprises an NPN type longitudinal bipolar transistor C and an NPN type longitudinal bipolar transistor D acting as said second longitudinal bipolar transistor;

collectors of said longitudinal bipolar transistors A, C are connected with said pad, bases thereof are connected with each other and emitters thereof are connected with a ground terminal;

said first resistor is connected between the bases of said longitudinal bipolar transistors A, C and said ground terminal;

collectors of said longitudinal bipolar transistors B, D are connected with an electric power source terminal, bases thereof are connected with each other and emitters thereof are connected with said pads;

said second resistor is connected between the bases of said longitudinal bipolar transistors B, D and said pads; and

at least either of said first resistor and said first longitudinal bipolar transistor or said second resistor and said second longitudinal bipolar transistor are provided.

13. The ESD protection apparatus according to Claim 11, wherein said pad is an electric power source terminal;

said first and second longitudinal bipolar transistors are NPN type and their collectors are connected with said pad and their bases are connected with each other and their emitters are connected with a ground terminal; and

a resistor is connected between the bases of said first and second longitudinal bipolar transistors and the ground terminal.

14. The ESD protection apparatus according to Claim 11, wherein said pad is an input terminal or an output terminal;

said trigger element comprises a PNP type longitudinal bipolar transistor A and a PNP type longitudinal bipolar transistor, B acting as said first longitudinal bipolar transistor, and a first and a second resistors;

said ESD protection element comprises a PNP type longitudinal bipolar transistor C and a PNP type longitudinal bipolar transistor D acting as said second longitudinal bipolar transistor;

emitters of said bipolar transistors A, C are connected with said pads, bases thereof are connected with each other and collectors thereof are connected with a ground terminal;

said first resistor is connected between the bases of said longitudinal bipolar transistors A, C and said pads;

emitters of said longitudinal bipolar transistors B, D are connected with an electric power source terminal, bases thereof are connected with each other and collectors thereof are connected with said pads;

said second resistor is connected between the bases of said longitudinal bipolar transistors B, D and said electric power source terminal; and

at least either of said first resistor and said first longitudinal bipolar transistor or said second resistor and said second longitudinal bipolar transistor are provided.

15. The ESD protection apparatus according to Claim 11, wherein said pad is an electric power source terminal;

said first and second longitudinal bipolar transistors are PNP type, and collectors thereof are connected with a ground

terminal, bases thereof are connected with each other and emitters thereof are connected with said pads; and

resistors are connected between the bases of said first and second longitudinal bipolar transistors and said pads.

16. The ESD protection apparatus according to Claim 11, wherein collector layers of said first longitudinal bipolar transistor and an emitter layers of said second longitudinal bipolar transistor are simultaneously formed.

17. The ESD protection apparatus according to Claim 11, wherein a collector layer of said first longitudinal bipolar transistor and an emitter layer of said second longitudinal bipolar transistor are a common layer.

18. The ESD protection apparatus according to Claim 1, wherein said longitudinal bipolar transistor or said diode comprises all or some of: a first $N^-$ type well formed on a P type silicon substrate surface; a second $N^-$ type well adjacent to the first $N^-$ type well and formed on said P type silicon substrate surface; a second $N^+$ layer formed on the second N-type well surface; a $P^-$ type well formed on said first $N^-$ type well surface; a $P^+$ layer and a first $N^+$ layer formed on the $P^-$ type well surface apart from each other; and an insulation material installed between the $P^+$ layer and the first $N^+$ layer for preventing an electric connection with said $P+^+$ layer and the first $N^+$ layer, and

said second $N^-$ type well and said $P^-$ type well are insulated by the insulation material for isolation, and said P type

silicon substrate and said $P^-$ type well are insulated by the insulation material for isolation.

19. The ESD protection apparatus according to Claim 1, wherein said longitudinal bipolar transistor or said diode comprises all or some of: a first $P^-$ type well formed on a N type silicon substrate surface; a second $P^-$ type well adjacent to the first $P^-$ type well and formed on said N type silicon substrate surface; a second $P^+$ layer formed on this second $P^-$ type well surface; a $N^-$ type well formed on said first $P^-$ type well surface; a $N^+$ layer and a first $P^+$ layer formed on the $N^-$ type well surface apart from each other; and an insulation material installed between the $N^+$ layer and the first $P^+$ layer for preventing the electric connection with said $P^+$ layer and first $N^+$ layer, and

said second $P^-$ type well and said $N^-$ type well are insulated by the insulation material for isolation, and said N type silicon substrate and said $N^-$ type well are insulated by the insulation material for isolation.

20. The ESD protection apparatus according to Claim 18, wherein said $P^+$ layer and said first and second $N^+$ layers are formed simultaneously with the $P^+$ layer and the $N^+$ layers of a CMOS transistor constituting said inner circuit.

21. The ESD protection apparatus according to Claim 19, wherein said $N^+$ layer and said first and second $P^+$ layers are formed simultaneously with the $N^+$ layers and the $P^+$ layer of the CMOS constituting said inner circuit.

22. The ESD protection apparatus according to the Claim 18, wherein said second $N^-$ type well is formed simultaneously with the $N^-$ type well of the CMOS transistor constituting said inner circuit.

23. The ESD protection apparatus according to the Claim 19, wherein said second $P^-$ type well is formed simultaneously with the $P^-$ type well of the CMOS transistor constituting said inner circuit.

24. The ESD protection apparatus according to Claim 18, wherein said insulation material is a dummy gate electrode or a simple insulation film formed simultaneously with a gate electrode and a gate insulation film of the CMOS transistor constituting said inner circuit.

25. The ESD protection apparatus according to Claim 24, wherein said dummy gate electrode or said insulation film is formed in a ring shape on said silicon substrate surface.

26. The ESD protection apparatus according to Claim 1, wherein said diode comprises: an $N^-$ type well formed on a P type silicon substrate surface; a $P^+$ layer and an $N^+$ layer formed on the $N^-$ type well surface apart from each other; and an insulation material formed inside from said P type silicon substrate surface between the $P^+$ layer and $N^+$ layer.

27. The ESD protection apparatus according to Claim 1, wherein said diode comprises: a $P^-$ type well formed on an N type silicon substrate surface; a $P^+$ layer and an $N^+$ layer formed on the $P^-$ type well surface apart from each other; and

an insulation material formed inside from said P type silicon substrate surface between the $P^+$layer and $N^+$layer.

28. The ESD protection apparatus according to Claim 1, wherein said diode comprises: an $N^-$type well formed on a P type silicon substrate surface; a $P^-$type well formed on the $N^-$type well surface; a $P^+$layer and $N^+$layer formed on the $P^-$type well surface apart from each other; and an insulation material installed on said P type silicon substrate surface between the $P^+$layer and $N^+$layer for preventing electric connection between said $P^+$layer and $N^+$layer, and

said P type silicon substrate and said $P^-$type well are insulated by the insulation material for isolation.

29. The ESD protection apparatus according to Claim 1, wherein said diode comprises: a $P^-$type well formed on an N type silicon substrate surface; an $N^-$type well formed on the $P^-$type well surface; a $P^+$layer and $N^+$layer formed on the $N^-$type well surface apart from each other; and an insulation material installed on said N type silicon substrate surface between the $P^+$layer and $N^+$layer for preventing electric connection between said $P^+$layer and $N^+$layer, and

said N type silicon substrate and said $N^-$type well are insulated by the insulation material for isolation.

30. The ESD protection apparatus according to Claim 1, wherein said diode comprises: a $P^-$type well formed on a silicon substrate surface; $N^+$layer and the $P^+$layer formed on the $P^-$type well surface apart from each other; and a dummy gate electrode installed on said $P^-$type well between the $N^+$layer

and $P^+$layer through an insulation film and connected with a ground terminal.

31. The ESD protection apparatus according to Claim 1, wherein said diode comprises: a $N^-$type well formed on a silicon substrate surface; $N^+$layer and the $P^+$layer formed on the $N^-$type well surface apart from each other; and a dummy gate electrode installed on said $N^-$type well between the $N^+$layer and $P^+$layer through an insulation film and connected with a ground terminal.

32. A method for fabricating an ESD protection apparatus according to Claim 1, comprising:

a first step of simultaneously forming an $N^-$ type well of a CMOS transistor composing said inner circuit and an $N^-$ type well for collector connection to be connected with the collector of said longitudinal bipolar transistor on a P type silicon substrate;

a second step of simultaneously forming a collector $N^-$ type well to be a collector of said longitudinal bipolar transistor and an $N^-$ type well of said diode on said P type silicon substrate;

a third step of simultaneously forming a $P^-$ type layer to be a base in the collector $N^-$ type well of said longitudinal bipolar transistor and a $P^-$ type layer to be an anode in the $N^-$ type well of said diode;

a fourth step of simultaneously forming an $N^+$ type layer in the $P^-$ type well of said CMOS transistor, an $N^+$ type layer in the $N^-$ type well for collector connection of said

longitudinal bipolar transistor, an $N^+$ type layer to be an emitter in the $P^-$ type layer of said longitudinal bipolar transistor, and an $N^+$ type layer to be a cathode in the $P^-$ type layer of said diode; and

a fifth step of simultaneously forming a $P^+$ type layer on the $N^-$ type well of said CMOS transistor, a $P^+$ type layer on the $P^-$ type layer of said longitudinal bipolar transistor, and a $P^+$ type layer on the $P^-$ type layer of said diode.

33. A method for fabricating the ESD protection apparatus according to Claim 2, comprising:

a first step of simultaneously forming an $N^-$ type well of a CMOS transistor constituting said inner circuit and the $N^-$ type well for collector connection to be connected with said longitudinal bipolar transistor on a P type silicon substrate;

a second step of simultaneously forming a collector $N^-$ type well to be a collector of said longitudinal bipolar transistor and the $N^-$ type well of said diode on said P type silicon substrate;

a third step of simultaneously forming a $P^-$ type layer to be a base in the collector $N^-$ type well of said longitudinal bipolar transistor and the $P^-$ type layer to be a cathode in the $N^-$ type well of said diode;

a fourth step of simultaneously forming an $N^+$ layer in the $P^-$ type well of said CMOS transistor, the $N^+$ layer in the $N^-$ type well for collector connection of said longitudinal bipolar transistor, the $N^+$ layer to be an emitter in the $P^-$ type

layer of said longitudinal bipolar transistor, and the $N^+$ layer to be an anode in the $P^-$ type layer of said diode; and

a fifth step of simultaneously forming the $P^+$ layer in the $N^-$ type well of said CMOS transistor, the $P^+$ layer in the $P^-$ type layer of said longitudinal bipolar transistor and the $P^+$ layer in the $P^-$ type layer of said diode.

34. The method for fabricating an ESD protection apparatus according to Claim 32, further comprising a step of forming a dummy gate electrode simultaneously with a gate electrode of said CMOS transistor in the region where the collector $N^-$ type well of said longitudinal bipolar transistor and $N^-$ type well of said diode are formed in said second step, wherein said dummy gate electrode is to prevent connection in the subsequent steps between the $N^+$ type layers of said longitudinal bipolar transistor and said diode formed in said fourth step and the $P^+$ type layers of said longitudinal bipolar transistor and said diode formed in the fifth step.

35. The method for fabricating an ESD protection apparatus according to Claim 32, further comprising a step of forming an insulation layer which prevents connection in the subsequent steps between the $N^+$ type layers of said longitudinal bipolar transistor and said diode formed in said fourth step and the $P^+$ type layers of said longitudinal bipolar transistor and said diode formed in the fifth step.

36. The method for fabricating an ESD protection apparatus according to Claim 32,

wherein an N replaces said conductive type P and a P replaces said conductive type N.

ADD A14